

respectfully requests reconsideration of the allowability of claims 1 - 23.

2. Claims 2, 11, 12, 18, and 19 have been rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. In particular, the Examiner stated that the phrase "at least one of" provides choices and is therefore unclear.

The applicant disagrees that the use of "at least one of" renders the claim indefinite. The phrase, as properly applied, is restricted to combinations within a given set of options. Thus, each combination of elements within the given set is disclosed and is therefore not indefinite. For instance, as used in claim 2, the given set includes an application and subroutines of an application. The "at least one of" phrase thus yields a definitive group of combinations. Those being: the application by itself, the subroutines by themselves, or both the application and subroutines. Accordingly, the applicant believes that the present rejection is overcome.

3. Claims 1, 2, 7-11, 14, 16, and 18 have been rejected under 35 USC § 102 (b) as being anticipated by Reents. In particular, the Examiner states that Figures 1 - 4 of Reents discloses a power efficient integrated circuit comprising a phase locked loop operably coupled to receive a reference clock and produce therefrom a system clock based on a system clock control, an on-chip power supply control module, a memory operably coupled to store at least

one application and a computational engine operably coupled to produce the system clock control signal and the power supply control signal based on processing transfer characteristics of the computational engine. The applicant respectfully disagrees with the Examiner's characterization of the present claims in view of the cited prior art.

Reents discloses an integrated circuit that has a core section having asynchronous partial resets. As Reents discloses in Figures 1 - 4, the integrated circuit 200 includes a core section 203 and two I/O driver sections 201 and 202, which include at least one driver circuit as shown in figure 4. The driver sections 201 and 202 are separately powered from the core and each other (column 6, lines 62 - 66). Power to the IC 200 is provided by power supply 206 via lines 207, 208, and 209. Switch 221 (figure 1), 306 (figure 2), or 419 (figure 3) is configured to provide power on one or more of the lines from the power supply 206, 300, or 413 to the IC 200 for entering and exiting power conservation mode. Figure 9 illustrates a method for entering power conservation mode.

As such, Reents does not disclose a phase lock loop (PLL) generating a system clock based on a system clock control signal, wherein the system clock control signal is generated based on the processing transfer characteristics of a computational engine and the processing requirements associated with processing an application. Reents discloses disabling the PLL entirely (column 8, lines 59 - 67) or disabling the output of the PLL (column 9, lines 10 - 13). As such, the Reents discloses that the PLL is either on or off based on the power conservation mode. In

contrast, the PLL has its operating rate, i.e., the generation of the system clock effected to converse power while in operation.

Reents does not teach or suggest an on-chip power supply control module as is presently claimed. Nor does Reents teach or suggest regulating at least one supply from a power source and an inductor based on a power supply control signal that is based on the processing transfer characteristics of a computational engine and the processing requirements associated with processing an application. Reents, however, discloses a separate power supply from the IC 200 as shown in Figures 1 - 3, where the supply lines are activated or deactivated based on the power conservation mode.

Reents does not teach or suggest having a computational engine generate the system clock control signal and the power supply control signal to converse power. As disclosed in the specification of the present application on page 10 at lines 24 - 26, by adjusting the system clock and/or the supply based on the application being executed by the IC, power consumption may be optimized.

Therefore, the applicant believes that claims 1, 2, 7-11, 14, 16, and 18 overcome the present rejection.

4. Claims 1, 2, 7-11, 14, 16, and 18 have been rejected under 35 USC § 102 (b) as being anticipated by Jackson. In particular, the Examiner states that Figures 3 and 6 of Reents discloses a power efficient integrated circuit

comprising a phase locked loop operably coupled to receive a reference clock and produce therefrom a system clock based on a system clock control, an on-chip power supply control module, a memory operably coupled to store at least one application and a computational engine operably coupled to produce the system clock control signal and the power supply control signal based on processing transfer characteristics of the computational engine. The applicant respectfully disagrees with the Examiner's characterization of the present claims in view of the cited prior art.

Jackson discloses a computer system 100 that includes a CPU 110, a clock generation circuit 160, and a power supply circuit 170. Jackson teaches that the supply circuit 170 includes a programmable regulator 172 and a switching regulator 171. The I/O controller 150 indicates the core voltage provided to the CPU by the programmable regulator 172. The switching regulator 171, however, is unaffected by the voltage modification control signal and continues to provide power to power plane of the computer system 100.

Jackson does not teach an integrated circuit that includes a PLL, an on-chip supply control module, memory, and a computational engine. In particular, the on-chip power supply control module, as claimed, regulates at least one supply for the IC from a power source and an inductor. Jackson teaches away from this, since Jackson teaches not affecting the switching regulator 171 when the power is to be conserved.

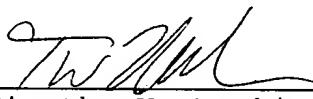
Therefore, the applicant believes that claims 1, 2, 7-11, 14, 16, and 18 overcome the present rejection.

5. For the foregoing reasdns, the applicant believes that claims 1 - 23 are in condition for allowance and respectfully request that they be passed to allowance.

6. The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

By:


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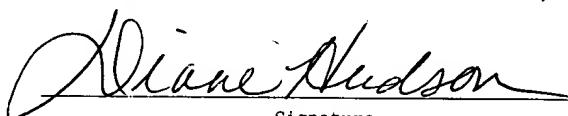
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